REMARKS

This communication is a request for reconsideration fully responsive to the Office Action dated February 5, 2008 and received in this application. Reconsideration and allowance of the pending claims in light of the following remarks is respectfully requested.

Claims 1-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,332,661 to Yamaguchi ("Yamaguchi") in view of U.S. Pat. No. 7,180,496 to Koyama et al. ("Koyama"). This rejection is traversed.

Claim 1 recites: *[a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,*

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object, each driver comprising

an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object and

a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.

These claimed features are neither disclosed nor suggested by the relied-upon references. Yamaguchi discloses a constant current driving semiconductor integrated circuit configured o drive a lot of loads by using constant current driver ICs in a state of small variations in output currents. A reference current generating circuit is embedded to derive a reference output current generated on a reference resistance from a reference output terminal. The Action readily admits that, and Yamaguchi makes no mention of, "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*," as claimed by Applicant.

Koyama does not remedy the deficiencies of Yamaguchi. Koyama discloses a drive circuit for driving a liquid crystal display device. However, in complete contrast to Applicant's claim 1 (and Yamaguchi), Koyama discloses a line driver circuit that outputs digital values (D1, D2, D3) to the pixel array in the form of a voltage. This digital line driver circuit of Koyama fails to even generally disclose the type of circuit claimed by Applicant, which is a "*current output type drive circuit for outputting a drive current ...comprising a plurality of drivers ... for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object.*"

Moreover, Koyama also clearly fails to disclose or suggest "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means,*" as claimed by Applicant. The Action cites FIG. 2, elements 201 and 202 as a purported example of this feature. However, these elements merely accommodate a latching of a digital signal (D1, D2, D3) that is then provided to a pixel circuit 205. At best, even if this is construed as "sampling" and "holding", the passing of a digital value D1, D2, or D3 to another circuit is clearly not an example of sampling a reference current input from a reference current input terminal. The passage cited in the Action (9:21-25) merely confirms that Koyama samples digital data, and in no way discloses or in any way suggests a reference current source circuit that samples and holds the reference current input from a reference current input terminal, and then supplies the same to the output means.

Accordingly, Koyama (1) discloses an entirely different type of circuit from that claimed by Applicant and (2) fails to disclose or in any way suggest the claimed features that the Action admits are absent from the Yamaguchi reference. With regard to the first issue, the line (voltage) driver circuit by Koyama is a clearly distinct from the current driver circuit claimed by Applicant. An ordinarily skilled artisan would in no way look to the latching of a digital value (D1-D3) for application to a line in a pixel circuit to solve problems presented in current drive circuitry. However, because of the second issue, even presuming the combination of these divergent circuits is appropriate (which is not the case), a *prima facie* case of obviousness remains absent from the

record as even the combination of references would still fail to yield the features of Applicant's claimed invention.

For these reasons, the combination of references is thus deficient generally, and the faulty combination still fails to produce the features recited in Applicant's claim 1.

Claims 3-6 depend from claim 1 and thus incorporate the features recited therein. These dependent claims are thus patentably distinct from the relied-upon references for their incorporation of the features of claim 1 as well as for their own, separately recited patentably distinct features.

The position with regard to these claims in the Action only further illustrates the impropriety of the combination as well as the deficiencies of the references, even in combination.

For example, claim 3 recites: ... *said current sampling circuit includes a first current memory and a second current memory, and said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory.* The Action cites elements A1 to A3 and B1 to B3 as the first current memory and elements C1 to C3 as the second current memory. However, these elements are part of the pixel, not a part of the line drive circuit. It is clear that these features are not an example of first and second current memories in a current sampling circuit, let alone those that alternately perform write and read operations as claimed.

Still further, with regard to claim 4, the relied-upon references offer no disclosure or suggestion of means for increasing the reference current read from the current memory via distribution by time division, and with regard to claim 5, there is clearly no disclosure or suggestion of the additional features for carrying out such an operation as clamed.

With regard to claim 6, there is also absolutely no discussion in Yamaguchi, as alleged in the Action, of distributing the reference current to the drivers in a vertical blanking period, or of

using as the reference current the current held after the vertical blanking period in which digital noise is generated, as claimed by Applicant.

The remaining independent claims 7, 22 and 23 are distinct for at least reasons similar to those provided regarding claim 1 above. Additionally, as noted above, with regard to claims 7 and 23 there is no disclosure or suggestion in the relied upon references of distributing the reference current to the reference current source circuits of the drivers by time division. The remaining claims depend from these claims and are thus distinct for incorporating the features therein as well as for their separately recited, distinct features, some of which are specifically addressed above.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-28 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi in view of Koyama.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of the claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests the Examiner to provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 18-0013, under Order No. SON-2815 from which the undersigned is authorized to draw.

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Respectfully submitted,

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